Total No. of Printed Pages:2

## SUBJECT CODE NO:- H-433 FACULTY OF SCIENCE AND TECHNOLOGY S.E. (CSE/IT) Digital Electronics (REVISED)

[Time: Three Hours] [Max.Marks: 80]

Please check whether you have got the right question paper.

- N.B 1. Q.1 and Q.6 are compulsory.
  - 2. Solve any two questions from Q.2 to Q.5 and any two questions from Q.7 to Q.10.

## **Section A**

Q.1 Solve any five questions:

10

- a) State and prove De-Morgan's theorem.
- b) Represent  $(-33)_{10}$  in
  - i) Sign Magnitude
  - ii) One's complement
- c) Convert following
  - i)  $(9 AC.FA)_{16} = (?)_8$
  - ii)  $(19.625)_{10} = (?)_2$
- d) Design a 4 i/p NAND gate by using 2 i/p NAND gates only.
- e) What is mean by self-complementing codes?
- f) Reduce following using k map.  $F(A, B, C) = \sum m (1,2,3,7)$
- g) Perform following binary arithmetic operations
  - i) (111 0101)/ (1001)
  - ii) (1001) \* (1101)
- h) Realize the following expression using logic gates  $Y = (\overline{A}.\overline{B}.\overline{C}) + (A \oplus B) + (A.C)$
- Q.2 a) Implement 3 input NAND gate using TTL logic.

07

b) Differentiate between analog signal and digital signal.

08

07

- Q.3 a) Define weighted codes, excess-3 code, BCD and define gray code. Explain with example.
  - b) Use NOR gate to produce AND, OR, NOT, NAND, X-OR and X-NOR gates.

08

1

## **Examination NOV/DEC 2018**

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Q.4	a)	Design binary to gray code converter.	07
	b)	What is digital signal? Explain its different characteristics.	08
Q.5	a)	Design a BCD to 7 segment decoder.	07
	b)	Design a 4 bit adder with look ahead carry.	08
		Section B	9,12 V
Q.6	a) b) c) d) e) f)	any five questions: What is Demultiplexer? Explain with any one example. Explain Decimal to BCD Encoder. What is PROM? What is the logic symbol and truth table of T F/F? Compare combinational and sequential circuits. Draw logic diagram for 4 bit PIPO shift reg. Draw 3 bit asynchronous counter. Write excitation table of SR F/F.	10
Q.7	a)	Design and implement circuit for 2 bit comparator using 4 line to 16 line decoder and multi input OR gates.	08
	b)	Draw and explain NAND implementation of 1 bit memory cell.	07
Q.8	a)	Design 16:1 multiplexer using two 8:1 multiplexer and logic gates. Explain working.	08
	b)	Draw logic diagram of 4 bit SISO right shift register. Explain it.	07
Q.9	a)	Convert i) SR F/F to JK F/F. ii) D type F/F to JK F/F	08
CELLO CO	b)	Design and explain MOD-10 ripple counter.	07
Q.10	a)	Explain designing of n bit comparator using IC.	08
	b)	Explain working of 4 bit universal shift register.	07