

**SUBJECT CODE NO:- P-142**  
**FACULTY OF ENGINEERING AND TECHNOLOGY**  
**S.E.(CSE/IT) Examination May/June 2017**  
**Digital Electronics**  
**(Revised)**

[Time:ThreeHours]

[Max.Marks:80]

Please check whether you have got the right question paper.

- N.B
- i) Q.No.1 and Q.No.6 are compulsory.
  - ii) Attempt any two questions from Q.2 to Q.5 and two question from Q.7 to Q.10

Section A

- Q.1 Solve any two question ( each for 2 marks ) 10
- a) What is along signal ?
  - b) What is dints care condition?
  - c) Draw 3 variable k-map
  - d) Draw symbol for x-or gate
  - e) Give truth table of or gate
  - f) What is PAL and PLA
  - g) Define prime implicant terms
  - h) What is decoder
- Q.2 07
- a) Explain logic gates in detail
  - b) Minimize following expression using k-map and realize the same using NAND gate only 08
- $Y ( A, B C D ) = \sum m ( 1, 4, 5, 6, 9, 12, 13, 14, ) + \sum d ( 8,10,11 )$
- Q.3 07
- a) Draw and explain 10 bit even parity generator
  - b) Minimize following logic expression using quine mc- cluskey method 08
- $F ( A, B, C, D ) = \sum m ( 0,1, 2, 3, 5, 7, 8, 9, 11, 14 )$
- Q.4 07
- a) Design 32:1 MUX using 8:1 MUX
  - b) Explain characteristics of digital ICs 08
- Q.5 08
- a) Realize following using 4 to 16 line decoder
- $f_1 = \sum m ( 0,3, 5, 6, 10, 11, 12 )$   
 $f_2 = \sum m ( 1, 2, 7, 13, 14, 15 )$   
 $f_3 = \sum m ( 2, 6, 10, 12, 13, 14 )$
- b) Compare combinational logic ckt with sequential logic ckt . 07

Section B

- Q.6 Solve any five question ( each for marks 2 ) 10
- a) Draw 4 bit PIPO shift register
  - b) Draw logic symbol of D flip – flop
  - c) Enlist types of shift register
  - d) What are the applications of DAC?
  - e) How many flip – flops are needed to design MOD 9 counter ?
  - f) Give truth table of T flip – flop
  - g) What us ring counter ?
  - h) What are the types of ADC?

- Q.7 a) draw and explain Johnson Ring counter 07  
b) Explain implementation of 3 bit R-2R binary ladder . 08
- Q.8 a) Explain single slop ADC 07  
b) Design 4 bit synchronous counter using D type flf 08
- Q.9 a) Convent S-R flf to D type flf and convent T f|f to D type f|f 08  
b) Draw and explain SISO right shift register 07
- Q.10 a) Design 3 bit parallel comparator ADC 07  
b) Explain UP- down counter 08